Precise Time-of-Flight Measurements Using a Novel High-Resolution Time-to-Digital Converter Architecture

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Time-to-digital converters (TDCs) are widely used for precise time-of-flight (ToF) measurements. They quantify the measured time interval T, corresponding to the travel time of the signal that is proportional to the distance from the target, and provide its digital value as a function of the time resolution. The proposed TDC architecture is able to provide very high resolution without averaging. Indeed, it virtually achieves a time resolution as fine as desired by simply increasing the self-timed ring oscillator (STRO) number of stages. In fact, the STRO is a multi-phase oscillator capable of providing one phase per stage output. The TDC exploits these different STRO phases, which are evenly spaced thanks to the unique analog STRO properties[1].

As a hardware proof-of-concept, this TDC, presented in Fig.1, has been implemented in a 0.35µm CMOS process[2] and a low-cost FPGA allowing ToF capture at a high repetitive rate to further confirm and evaluate the advantages of our proposed TDC architecture. Three TDCs with L = 9, 23, and 61 have been integrated on the same ASIC 0.35µm CMOS technology chip. Most of the measurements are in accordance with our theoretical claims. The fabricated circuits prove the ability of this TDC to enhance the time resolution by increasing the number of stages. Indeed, the smallest TDC, with L = 9, samples the time intervals with a time resolution of 72.5 ps, while a time resolution of 13.9 ps is obtained with the TDC of L = 61. On the other hand, a 23-stage and 141-stage STRO-based TDC have been implemented in a low-cost Cyclone IV FPGA. A 20.0 ps time resolution has been achieved using 141 stages with measured DNL and INL of 1.88 LSB and 2.24 LSB, respectively, obtained in a one-shot measurement without averaging. This work highlights the advantages of this new TDC in terms of measurement accuracy, calibration, low cost, on-the-fly measurements, and simplicity of implementation. Therefore, it is highly suitable for a ToF architecture.

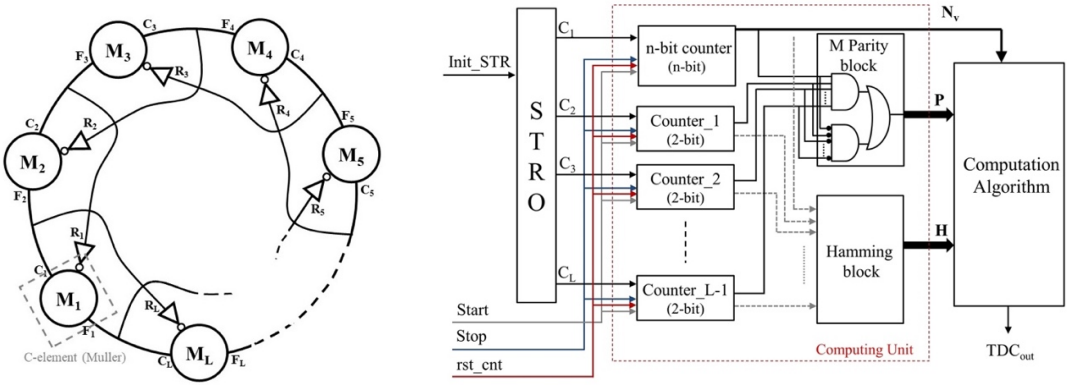

Fig. 1: STRO Architecture of L-stages and the proposed TDC architecture using L-stage STRO.

[1]A. El-Hadbi *et al.*, "An accurate *TDC* based on a *STRO* for on-the-fly time measurement," AICSP, vol. 97, 2018.
[2]A. El-Hadbi *et al.*, "*STRO* based *TDC*: A 0.35µ m CMOS *PoC* Prototype," IEEE I2MTC'21, Glasgow, UK, 2021.

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